CLAIMS

What is claimed is:

1.   A method comprising:
searching an associative memory cache using a search key;
in response to a miss at the associative memory cache, accessing a primary associative
       memory;
identifying in the primary associative memory an entry matching the search key and a
       number of overlapping entries; and
creating a non-overlapping entry, the non-overlapping entry having a range that includes
       at least a portion of a range of the matching entry and that does not include ranges
       of the overlapping entries.

2.   The method of claim 1, wherein the matching entry comprises a highest
priority matching entry.

3.   The method of claim 1, wherein the range of the non-overlapping entry
includes the largest possible portion of the range of the matching entry.

4.   The method of claim 1, further comprising entering the non-overlapping
entry into the associative memory cache.

5.   The method of claim 4, further comprising:
identifying an existing entry in the associative memory cache for replacement; and
replacing the identified existing entry with the non-overlapping entry.

6.   The method of claim 1, wherein creating the non-overlapping entry
comprises:
determining a comparand for the non-overlapping entry; and
using a priority of the matching entry as a priority of the non-overlapping entry.

1   7.   The method of claim 6, wherein creating the non-overlapping entry further

2 comprises using data associated with the matching entry as data associated with the non-

3 overlapping entry.

1   8.   The method of claim 6, wherein determining the comparand for the non-

2 overlapping entry comprises determining a binary range.

1   9.   The method of claim 8, wherein the associative memory cache comprises

2 a ternary content addressable memory (CAM).

1   10.   The method of claim 6, wherein determining the comparand for the non-

2 overlapping entry comprises determining a non-binary range.

1   11.   The method of claim 10, wherein the associative memory cache comprises

2 a boundary addressable memory (BAM).

1   12.   The method of claim 6, wherein determining the comparand for the non-

2 overlapping entry comprises using the search key as the comparand.

1   13.   The method of claim 12, wherein the associative memory cache comprises

2 a binary CAM.

1　　　　　14.　An apparatus comprising:

2　an associative memory cache;

3　a primary associative memory;

4　a cache control coupled with each of the associative memory cache and the primary

5　　　　　associative memory, the cache control to search the associative memory cache

6　　　　　using a search key and, in response to a miss, access the primary associative

7　　　　　memory to identify an entry matching the search key and a number of overlapping

8　　　　　entries; and

9　a conversion module coupled with the cache control, the conversion module to create a

10　　　　　non-overlapping entry, the non-overlapping entry having a range that includes at

11　　　　　least a portion of a range of the matching entry and that does not include ranges of

12　　　　　the overlapping entries.

1　　　　　15.　The apparatus of claim 14, wherein the matching entry identified by the

2　cache control comprises a highest priority matching entry.

1　　　　　16.　The apparatus of claim 14, further comprising a search client coupled with

2　the cache control, the search client to issue a search request to the cache control, the

3　search request including the search key.

1　　　　　17.　The apparatus of claim 14, further comprising replacement logic coupled

2　with the cache control, the replacement logic to select an existing entry in the associative

3　memory cache for replacement by the non-overlapping entry.

1　　　　　18.　The apparatus of claim 14, wherein to create the non-overlapping entry,

2　the conversion module determines a comparand for the non-overlapping entry and uses a

3　priority of the matching entry as a priority of the non-overlapping entry.

1   19.   The apparatus of claim 18, wherein to create the non-overlapping entry,

2   the conversion module uses data associated with the matching entry as data associated

3   with the non-overlapping entry.

1   20.   The apparatus of claim 18, wherein the comparand comprises one of a

2   binary range and a non-binary range.

1   21.   The apparatus of claim 14, further comprising a second associative

2   memory cache coupled with the cache control.

1   22.   The apparatus of claim 14, wherein the associative memory cache, the

2   primary associative memory, the cache control, and the conversion module are located on

3   a single integrated circuit device.

1   23.   The apparatus of claim 14, wherein the associative memory cache

2   comprises an off-chip associative memory.

1   24.   The apparatus of claim 14, wherein the primary associative memory

2   comprises an off-chip associative memory.

1   25.   The apparatus of claim 14, wherein the associative memory cache

2   comprises one of a binary content addressable memory (CAM), a ternary CAM, and a

3   boundary addressable memory (BAM).

1   26.   The apparatus of claim 14, wherein the primary associative memory

2   comprises one of a ternary CAM and a BAM.

1   27.   The apparatus of claim 14, wherein the primary associative memory

2   comprises:

3   a memory; and

4   a search engine coupled with the memory and the cache control, the search engine

5   including an algorithm to utilize the memory as an associative memory.

1   28.   The apparatus of claim 27, wherein the memory comprises one of a static

2   random access memory (SRAM) and a dynamic random access memory (DRAM).

1   29.   The apparatus of claim 27, wherein the memory comprises an off-chip

2   memory.

1   30.   A network processor comprising:

2   an associative memory cache;

3   a search engine coupled with a dynamic random access memory (DRAM), the search

4   engine including an algorithm to utilize the DRAM as an associative memory;

5   a cache control coupled with each of the associative memory cache and the search

6   engine, the cache control to search the associative memory cache using a search

7   key and, in response to a miss, access the DRAM to identify an entry matching

8   the search key and a number of overlapping entries; and

9   a conversion module coupled with the cache control, the conversion module to create a

10   non-overlapping entry, the non-overlapping entry having a range that includes at

11   least a portion of a range of the matching entry and that does not include ranges of

12   the overlapping entries.

1   31.   The network processor of claim 30, wherein the matching entry identified

2   by the cache control comprises a highest priority matching entry.

1   32.   The network processor of claim 30, further comprising a search client
2   coupled with the cache control, the search client to issue a search request to the cache
3   control, the search request including the search key.

1   33.   The network processor of claim 30, wherein the search key is received
2   from an off-chip search client.

1   34.   The network processor of claim 30, further comprising replacement logic
2   coupled with the cache control, the replacement logic to select an existing entry in the
3   associative memory cache for replacement by the non-overlapping entry.

1   35.   The network processor of claim 30, wherein to create the non-overlapping
2   entry, the conversion module determines a comparand for the non-overlapping entry and
3   uses a priority of the highest priority matching entry as a priority of the non-overlapping
4   entry.

1   36.   The network processor of claim 35, wherein to create the non-overlapping
2   entry, the conversion module uses data associated with the highest priority matching
3   entry as data associated with the non-overlapping entry.

1   37.   The network processor of claim 35, wherein the comparand comprises one
2   of a binary range and a non-binary range.

1   38.   The network processor of claim 30, further comprising a second
2   associative memory cache coupled with the cache control.

1   39.   The network processor of claim 38, wherein the second associative
2   memory cache comprises an off-chip associative memory.

1   40.   The network processor of claim 30, wherein the associative memory cache

2   comprises one of a binary content addressable memory (CAM), a ternary CAM, and a

3   boundary addressable memory (BAM).

1   41.   The network processor of claim 30, wherein the DRAM comprises part of

2   the network processor.

1   42.   An article of manufacture comprising:

2   a machine accessible medium providing content that, when accessed by a machine,

3   causes the machine to

4   search an associative memory cache using a search key;

5   in response to a miss at the associative memory cache, access a primary

6   associative memory;

7   identify in the primary associative memory an entry matching the search key and

8   a number of overlapping entries; and

9   create a non-overlapping entry, the non-overlapping entry having a range that

10   includes at least a portion of a range of the matching entry and that does

11   not include ranges of the overlapping entries.

1   43.   The article of manufacture of claim 42, wherein the matching entry

2   comprises a highest priority matching entry.

1   44.   The article of manufacture of claim 42, wherein the range of the non-

2   overlapping entry includes the largest possible portion of the range of the matching entry.

1   45.   The article of manufacture of claim 42, wherein the content, when

2   accessed, further causes the machine to enter the non-overlapping entry into the

3   associative memory cache.

1   46.   The article of manufacture of claim 45, wherein the content, when

2   accessed, further causes the machine to:

3   identify an existing entry in the associative memory cache for replacement; and

4   replace the identified existing entry with the non-overlapping entry.

1   47.   The article of manufacture of claim 42, wherein the content, when

2   accessed, further causes the machine, when creating the non-overlapping entry, to:

3   determine a comparand for the non-overlapping entry; and

4   use a priority of the matching entry as a priority of the non-overlapping entry.

1   48.   The article of manufacture of claim 47, wherein the content, when

2   accessed, further causes the machine, when creating the non-overlapping entry, to use

3   data associated with the matching entry as data associated with the non-overlapping

4   entry.

1   49.   The article of manufacture of claim 47, wherein the comparand comprises

2   one of a binary range and a non-binary range.